TRANSMITTAL OF APPEAL BRIEF

Docket No.
SON-1199/DIV

In re Application of: Hideaki KURODA

Application No.	Filing Date	Examiner	Group Art Unit
09/866,662	May 30, 2001	M. V. Prenty	2822

Invention: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

TO THE COMMISSIONER OF PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application.

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Dated: March 10, 2004

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SCN-1199/CON2
(80001-2149)

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Hideaki KURODA

Examiner: M. V. Prenty

Art Unit: 2822

Application No.: 09/866,662

Filed: May 30, 2001

Confirmation No.: 6271

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

APPELLANT'S BRIEF

MS APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This brief is in furtherance of the Notice of Appeal, filed in this case on February 10, 2004.

The fees required under § 1.17(f) and any required petition for extension of time for filing this brief and fees therefor, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief is transmitted in triplicate.

This brief contains items under the following headings as required by 37 C.F.R. § 1.192 and M.P.E.P. § 1206:

I. Real Party In Interest
II Related Appeals and Interferences
III. Status of Claims
IV. Status of Amendments
V. Summary of Invention
VI. Issues
VII. Grouping of Claims
VIII. Arguments
IX. Claims Involved in the Appeal
Appendix A. Claims on Appeal
Appendix B. Copies of Figs. 2, 3, and 17

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

The Sony Corporation of Tokyo, Japan. An assignment of all rights in the present application to The Sony Corporation of Tokyo, Japan was executed by the inventor and recorded by the U.S. Patent and Trademark Office on **reel 8878** at **frame 0561.**

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 4 claims pending in this application. Claims 3-6 stand twice rejected and no claims are currently allowed. The Appellant hereby appeals the final rejection of claims 3-6, which are presented in Appendix A.

B. Current Status of Claims

1. Claims canceled: 1, 2, and 7-22.
2. Claims withdrawn from consideration but not canceled: None
3. Claims pending: 3-6
4. Claims allowed: None
5. Claims rejected: 3-6

C. Claims On Appeal

The claims on appeal are claims 3-6.

IV. STATUS OF AMENDMENTS

The instant application was filed on May 30, 2001 concurrently with a preliminary amendment in which claim 3 was amended to include the subject matter of claim 1, claim 4 was amended to include the subject matter of claims 1 and 2, and claims 5 and 6 were

amended to improve idiomatic English. On February 5, 2003, and in response to a non-final Office Action dated June 14, 2002, an amendment to claims 3 and 4 was made to improve form. On July 25, 2003 and in response to a final Office Action dated July 15, 2003, a Request for Continued Examination was filed along with a Preliminary Amendment in which claims 3 and 4 were amended to further distinguish the invention over the prior art. On November 6, 2003 and in response to a non-final Office Action dated August 2, 2003, an amendment to the specification was filed. No response was filed subsequent to the final Office Action dated December 10, 2003 (Paper No. 16), which is the subject of this appeal.

Accordingly, the claims enclosed herewith as Appendix A incorporate the amendments indicated in the paper filed by Appellant on July 25, 2003.

V. SUMMARY OF INVENTION

Independent claim 3 recites a semiconductor device comprising, a conductive layer pattern (214a, 214b) formed on a substrate (211); a first inter-layer insulating film (215) which covers said conductive layer pattern (214a, 214b) and is formed on said substrate (211); a first connection hole (216) formed in a upper layer of said first inter-layer insulating film (215) above said conductive layer pattern (214a); a second connection hole (217) which reaches said conductive layer pattern (214a) from the bottom portion of said first connection hole (216) and then has a smaller diameter than that of said first connection hole (216) and formed on said first inter-layer insulation film (215); a plug (218) having conductivity and filling internal portions of said first connection hole (216) and said second connection hole (217); a second inter-layer insulating film (219) formed on said first inter-layer insulating film (215), wherein said second inter-layer insulating film (219) includes up to five layers; a third connection hole (220) which reaches said plug (218) and is formed through said second inter-layer insulating film (219); and a conductive portion (221) which is connected to said plug (218) and formed in said third connection hole (220). *See* page 17 line 8 through page 20 line 11.

Independent claim 4 recites a semiconductor device, comprising a conductive layer pattern (214a, 214b) formed on a substrate (211); a first inter-layer insulating film (215) which covers said conductive layer pattern (214a, 214b) and is formed on said substrate (211); a first connection hole (216) formed in a upper layer of said first inter-layer insulating film (215) above said conductive layer pattern (214a); a second connection hole (217) which

reaches said conductive layer pattern (214a) from the bottom portion of said first connection hole (216) and then has a smaller diameter than that of said first connection hole (216) and formed on said first inter-layer insulation film (215); a plug (218) having conductivity and filling internal portions of said first connection hole (216) and said second connection hole (217), wherein the upper surface of said plug (218) is formed to almost the same height as the surface height of said first inter-layer insulating film (215); a second inter-layer insulating film (219) formed on said first inter-layer insulating film (215), wherein said second inter-layer insulating film (219) includes up to five layers; a third connection hole (220) which reaches said plug (218) and is formed through said second inter-layer insulating film (219); and a conductive contact portion (221) which is connected to said plug (218) and formed in said third connection hole (220). *See* page 17 line 8 through page 20 line 11.

VI. ISSUES

The issue presented for appeal in this application is as follows:

Whether the Examiner erred in rejecting claims 3-6 under 35 U.S.C. §102 as anticipated by *Applicant's Alleged Admitted Prior Art Fig. 3* (*Fig. 3*).

VII. GROUPING OF CLAIMS

For purposes of this appeal brief only, and without conceding the teachings of any prior art reference, the claims have been grouped as indicated below:

Claims 3-6 stand or fall together with respect to the §102 rejection over *Fig. 3.*

VIII. ARGUMENTS

In the final Office Action dated December 10, 2003 (Paper No. 16), the Examiner expressed the following claim rejection:

Claims 3-6 were rejected under 35 U.S.C. §102 as anticipated by *Applicant's Alleged Admitted Prior Art Fig. 3* (*Fig. 3*).

For at least the reasons set forth below, the aforementioned claim rejections are technically and legally unsound. Accordingly, the §102 rejections should be reversed.

Independent claim 3 recites a semiconductor device comprising, a conductive layer pattern formed on a substrate; a first inter-layer insulating film which covers said conductive layer pattern and is formed on said substrate; a first connection hole formed in a upper layer

of said first inter-layer insulating film above said conductive layer pattern; a second connection hole which reaches said conductive layer pattern from the bottom portion of said first connection hole and then has a smaller diameter than that of said first connection hole and formed on said first inter-layer insulation film; a plug having conductivity and filling internal portions of said first connection hole and said second connection hole; a second inter-layer insulating film formed on said first inter-layer insulating film, wherein said second inter-layer insulating film includes up to five layers; a third connection hole which reaches said plug and is formed through said second inter-layer insulating film; and a conductive portion which is connected to said plug and formed in said third connection hole.

Independent claim 4 recites a semiconductor device, comprising a conductive layer pattern formed on a substrate; a first inter-layer insulating film which covers said conductive layer pattern and is formed on said substrate; a first connection hole formed in a upper layer of said first inter-layer insulating film above said conductive layer pattern; a second connection hole which reaches said conductive layer pattern from the bottom portion of said first connection hole and then has a smaller diameter than that of said first connection hole and formed on said first inter-layer insulation film; a plug having conductivity and filling internal portions of said first connection hole and said second connection hole, wherein the upper surface of said plug is formed to almost the same height as the surface height of said first inter-layer insulating film; a second inter-layer insulating film formed on said first inter-layer insulating film, wherein said second inter-layer insulating film includes up to five layers; a third connection hole which reaches said plug and is formed through said second inter-layer insulating film; and a conductive contact portion which is connected to said plug and formed in said third connection hole.

Fig. 2 illustrates a plan view of a conventional COP type DRAM cell. This DRAM cell includes, among other things, gate electrodes 51a–51d, bit contact 52, bit lines 53a-53c, and node contacts 54a-54d. Further, *Fig. 2* includes a line A-A', which corresponds to a sectional view illustrated in Fig. 3, and line B-B', which corresponds to a sectional view illustrated in *Fig. 17.*

Fig. 3 illustrates a first cut-away view of the COP type DRAM cell illustrated in Fig. 2 along line A-A', which traverses along the center of node contacts 54a and 54c. The cut-away view of *Fig. 3* is shown as if one were viewing the DRAM cell of *Fig. 2* in a longitudinal direction from the left side to the right side. As a matter of convenience,

Appellant has attached a marked-up drawing of *Fig. 3* in Appendix B. As shown in the drawing, the top layer of the DRAM cell includes node contact 54c on the left, bit contact 52 in the middle, and node contact 54a on the right, which corresponds to like numbered elements shown in *Fig. 2*. Directly below the aforementioned top layer and between layers 164 and 154, *Fig. 3* shows three bit lines BL. The bit line BL positioned on the left corresponds to bit line 53c shown in *Fig. 2*. Further, the bit line BL positioned in the center and below bit contact 52 corresponds to bit line 53b shown in *Fig. 2*. Still further, the bit line BL positioned on the right corresponds to bit line 53a shown in *Fig. 2*. The Office Action alleges the portion of the DRAM cell shown in *Fig. 3* that includes the three bit lines BL is the second-interlayer insulating film. Appellant disagrees because the bit lines BL are buried within the second interlayer insulating film. In this manner, the layers comprising the second interlayer insulating film includes those layers that make up the bit line. Based on this reasoning, and from the example provided in Fig. 3 the second interlayer insulating film includes eight layers.

Still further, the layers making up the bit lines cannot be included in determining the number of layers that make-up the second interlayer insulating film for the reasons that follow.

Fig. 17 illustrates a second cut-away view of the COP type DRAM cell illustrated in Fig. 2 along line B-B', which traverses the DRAM cell diagonally in a longitudinal direction passing through the center of node contacts 54a and 54d, and bit contact 54a. The cut-away view of *Fig. 3* is shown as if one were viewing the DRAM cell of Fig. 2 in a widthwise direction, which is the same direction in which line A-A' is cut. As a matter of convenience, Appellant has attached a marked-up drawing of *Fig. 17* in Appendix B. As shown in *Fig. 17*, node contacts 54a and 54d and bit contact 54a are all embedded within layer 167. In particular, node contact 54a is shown on the left edge of the DRAM cell, bit contact 52 is located adjacent to node contact 54a and spaced a specified distance from node contact 54a, and node contact 54d is adjacent to bit contact 52 and spaced a specified distance from node bit contact 52. As a result of the direction along which line B-B' is cut, only one bit line BL is shown in *Fig. 17*. This bit line is located beneath the bit contact 52 and corresponds to bit line 53b as shown in *Fig. 2*. The second interlayer insulating film is identified by the bracket on the marked-up copy of the drawing. The portions of second interlayer insulating film shown below node contacts 54a and 54d do not include embedded bit lines. However, even

without the bit lines the second interlayer insulating film is depicted as having more than five layers. It follows, therefore, that *Fig. 17* does not anticipate the claimed invention.

In summary, claims 3 and 4 recite that the second inter-layer insulating film includes up to five layers. The conventional DRAM cell as illustrated in related prior art figures 2, 3, and 17, has a second inter-layer insulating film that includes more than five layers. To properly anticipate a claim, the document must disclose, explicitly or implicitly, each and every feature recited in the claim. *See* Verdegall Bros. v. Union Oil Co. of Calif., 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Because the prior art figures, and in particular *Fig. 3*, fail to disclose, teach, or suggest every element recited in claims 3 and 4, Appellant respectfully submits that claims 3 and 4 are not anticipated. Accordingly, Appellant requests that the rejection of claims 3 and 4 not be sustained.

Claims 5 depends from claim 3 and claim 6 depends from claim 4. By virtue of this dependency, Appellant submits that claims 5 and 6 are allowable for at least the same reasons given above concerning claims 3 and 4, respectively. In addition, Appellant submits that claims 5 and 6 are further distinguished over *Fig. 3* by the additional elements recited therein, and particularly with respect to each claimed combination. Appellant respectfully requests, therefore, that the rejection of claims 5 and 6 under 35 U.S.C. §102 not be sustained.

For at least the foregoing reasons, Appellant submits that the final rejection of claims 3-6 is improper and should not be sustained. Therefore, concerning claims 3-6, Appellant respectfully requests reversal of the final rejection dated December 10, 2003 (Paper No. 16).

IX. CLAIMS INVOLVED IN THE APPEAL

A copy of the claims involved in the present appeal is attached hereto in Appendix A.

Appellant has authorized that Deposit Account No. 18-0013 be charged for the fee due with this response. However, if any additional fee is due, please charge our Deposit Account No. 18-0013, under Order No. SON-1199/DIV from which the undersigned is authorized to draw.

Dated: March 10, 2004

Respectfully submitted,

By 
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In the event additional fees are necessary in connection with the filing of this paper, or if a petition for extension of time is required for timely acceptance of same, the Commissioner is hereby authorized to charge Deposit Account No. 180013 for any such fees; and applicants hereby petition for any needed extension of time.

APPENDIX A

Claims Involved in the Appeal of Application Serial No. 09/866,662

A copy of the claims involved in the present appeal is set forth below:

3. (PREVIOUSLY PRESENTED) A semiconductor device, comprising:

a conductive layer pattern formed on a substrate;

a first inter-layer insulating film which covers said conductive layer pattern and is formed on said substrate;

a first connection hole formed in a upper layer of said first inter-layer insulating film above said conductive layer pattern;

a second connection hole which reaches said conductive layer pattern from the bottom portion of said first connection hole and then has a smaller diameter than that of said first connection hole and formed on said first inter-layer insulation film;

a plug having conductivity and filling internal portions of said first connection hole and said second connection hole;

a second inter-layer insulating film formed on said first inter-layer insulating film, wherein said second inter-layer insulating film includes up to five layers;

a third connection hole which reaches said plug and is formed through said second inter-layer insulating film; and

a conductive portion which is connected to said plug and formed in said third connection hole.

4. (PREVIOUSLY PRESENTED) A semiconductor device, comprising:

a conductive layer pattern formed on a substrate;

a first inter-layer insulating film which covers said conductive layer pattern and is formed on said substrate;

a first connection hole formed in a upper layer of said first inter-layer insulating film above said conductive layer pattern;

a second connection hole which reaches said conductive layer pattern from the bottom portion of said first connection hole and then has a smaller diameter than that of said

first connection hole and formed on said first inter-layer insulation film;

a plug having conductivity and filling internal portions of said first connection hole and said second connection hole, wherein the upper surface of said plug is formed to almost the same height as the surface height of said first inter-layer insulating film;

a second inter-layer insulating film formed on said first inter-layer insulating film, wherein said second inter-layer insulating film includes up to five layers;

a third connection hole which reaches said plug and is formed through said second inter-layer insulating film; and

a conductive contact portion which is connected to said plug and formed in said third connection hole.

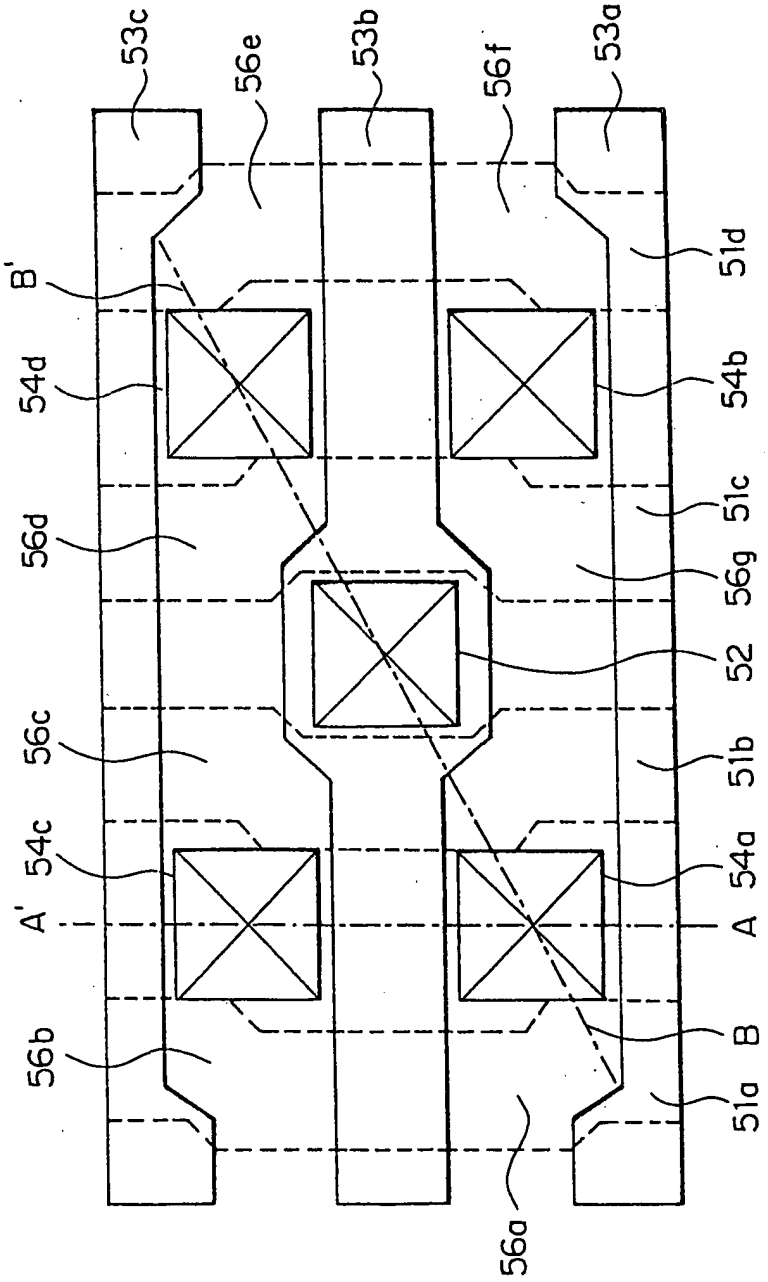
5. (ORIGINAL) A semiconductor device according to claim 3, wherein said plug and said conductive portion are a storage node contact portion of a dynamic random access memory.

6. (ORIGINAL) A semiconductor device according to claim 4, wherein said plug and said conductive portion are a storage node contact portion of a dynamic random access memory.

APPENDIX B

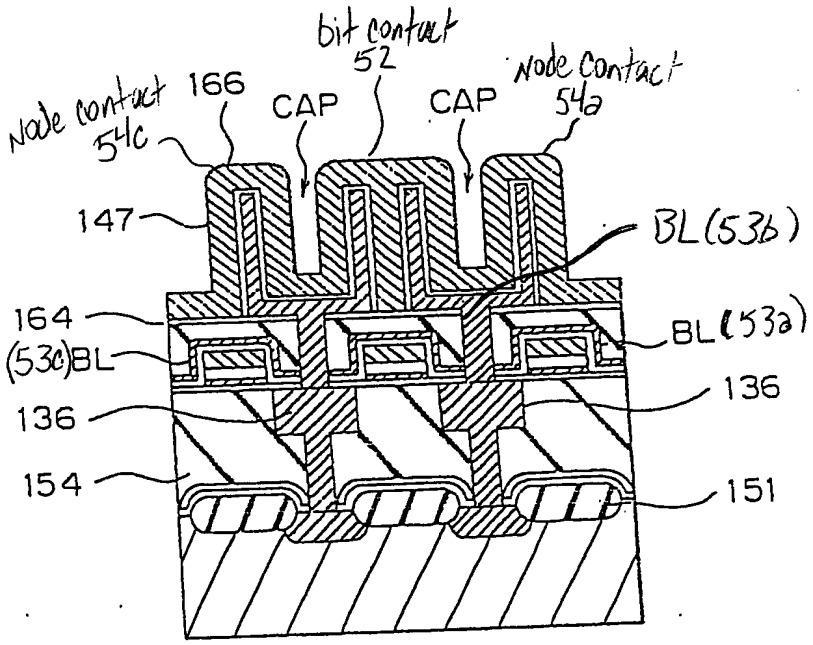
Marked up copies of Figs. 2, 3, and 17.

FIG. 2



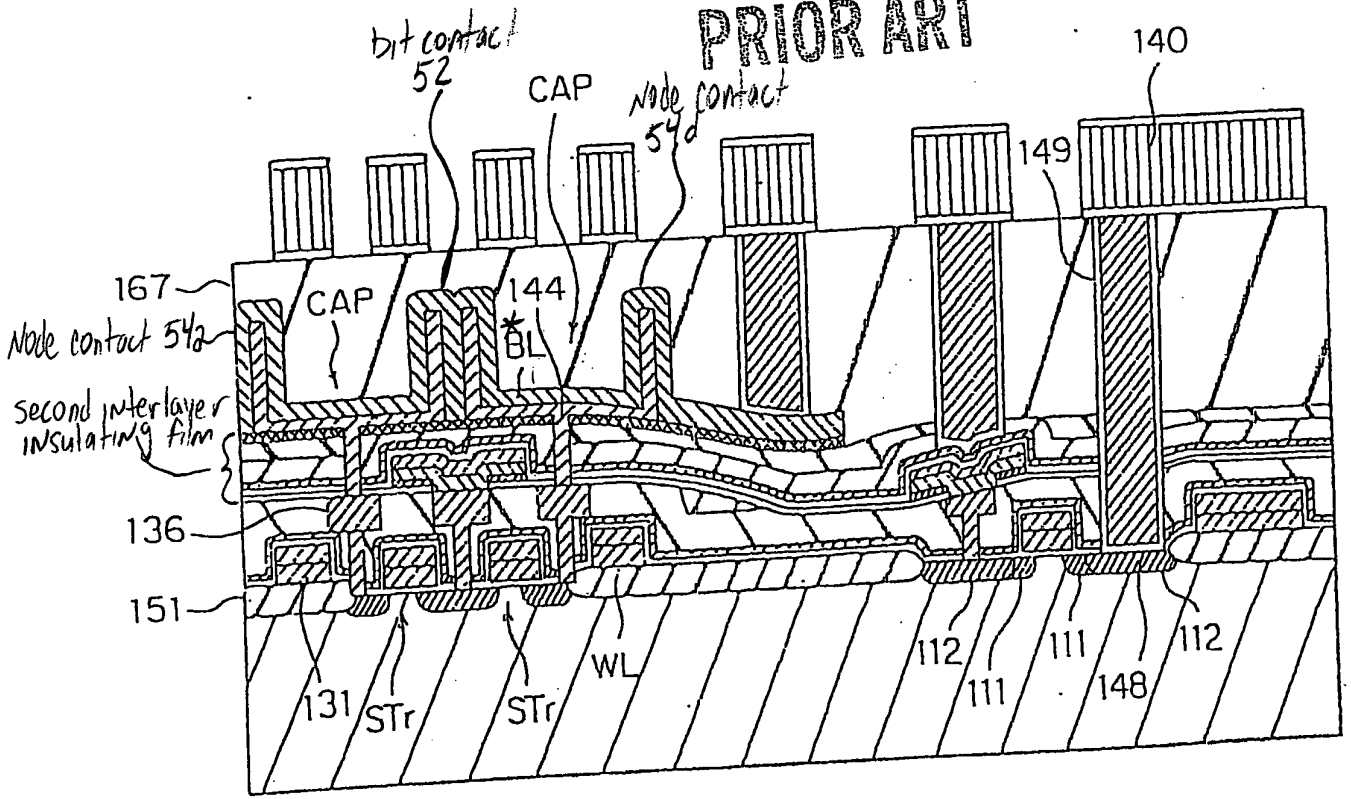
PRIOR ART

FIG. 3



PRIOR ART

FIG. 17
PRIOR ART



* Bit line BL corresponds to bit line 53b of Fig. 2.